

On-chip multi-sorting using flow path switching by local-flow control

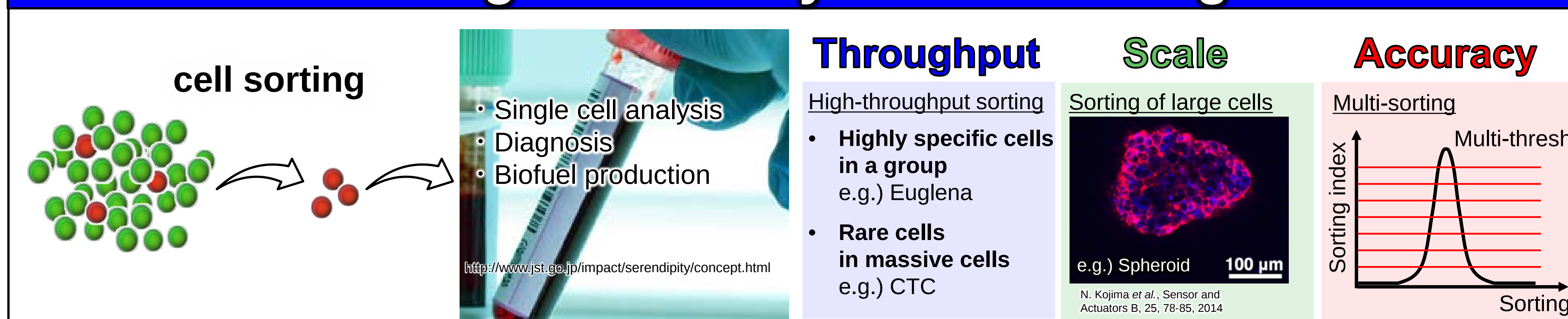
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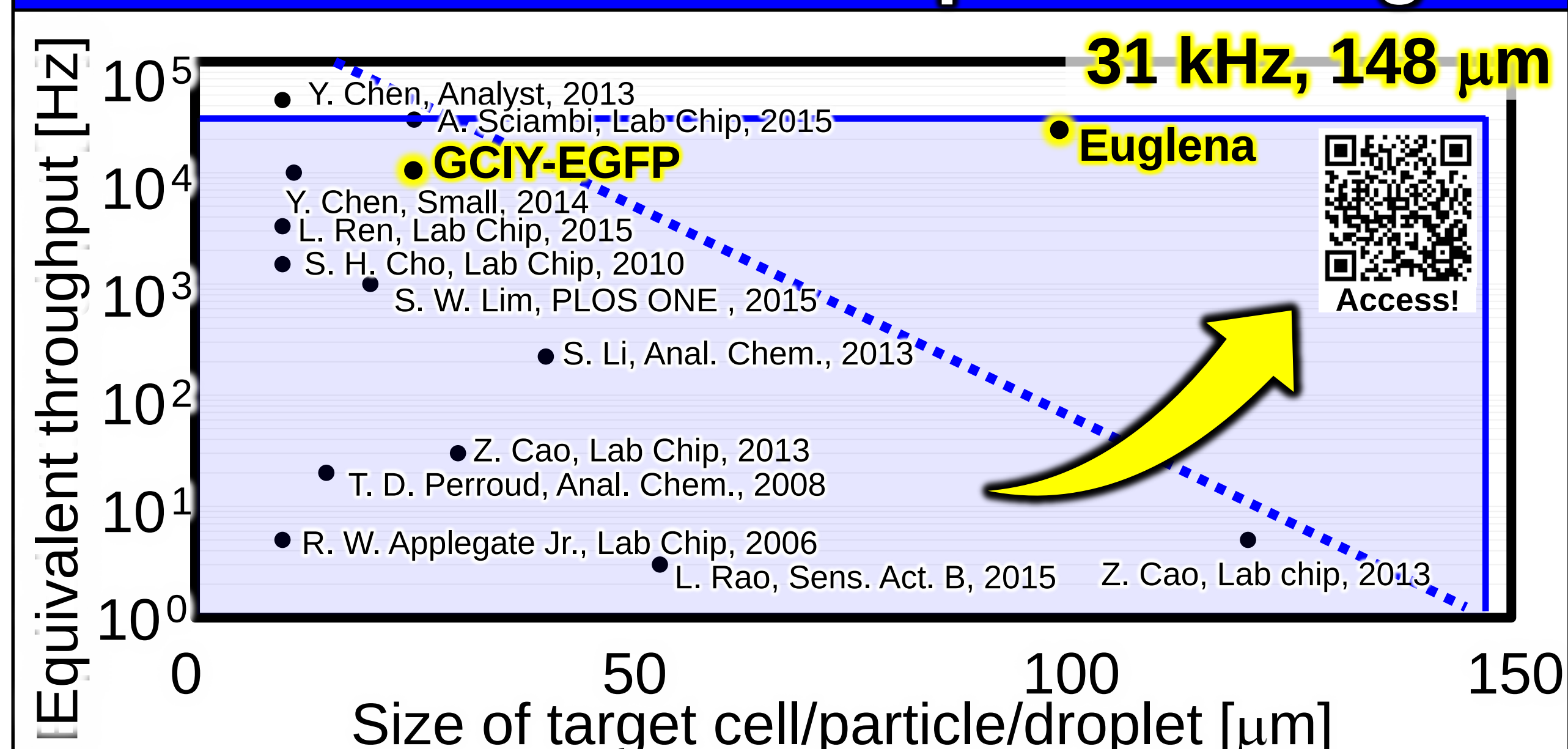


High-speed, high-precision, and multi-scale on-chip flow control

Background & keys of cell sorting



Benchmark of on-chip cell sorting



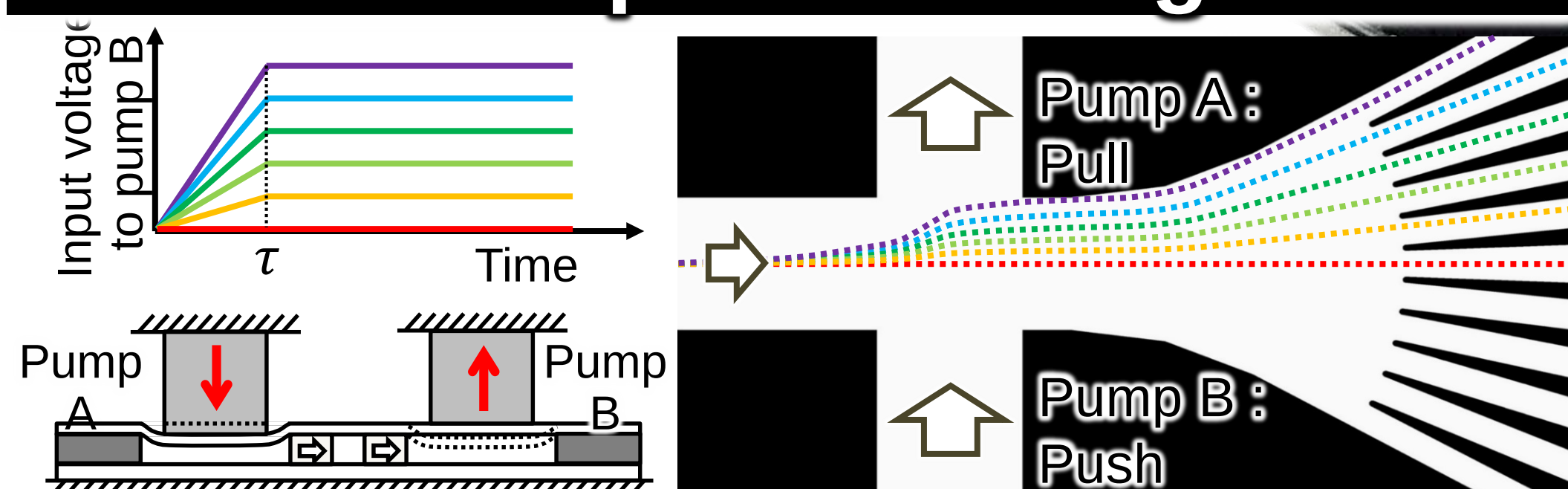
On-chip dual membrane pumps

Piezoelectric actuator
Attachment
Glass membrane
High-rigidity microfluidic chip

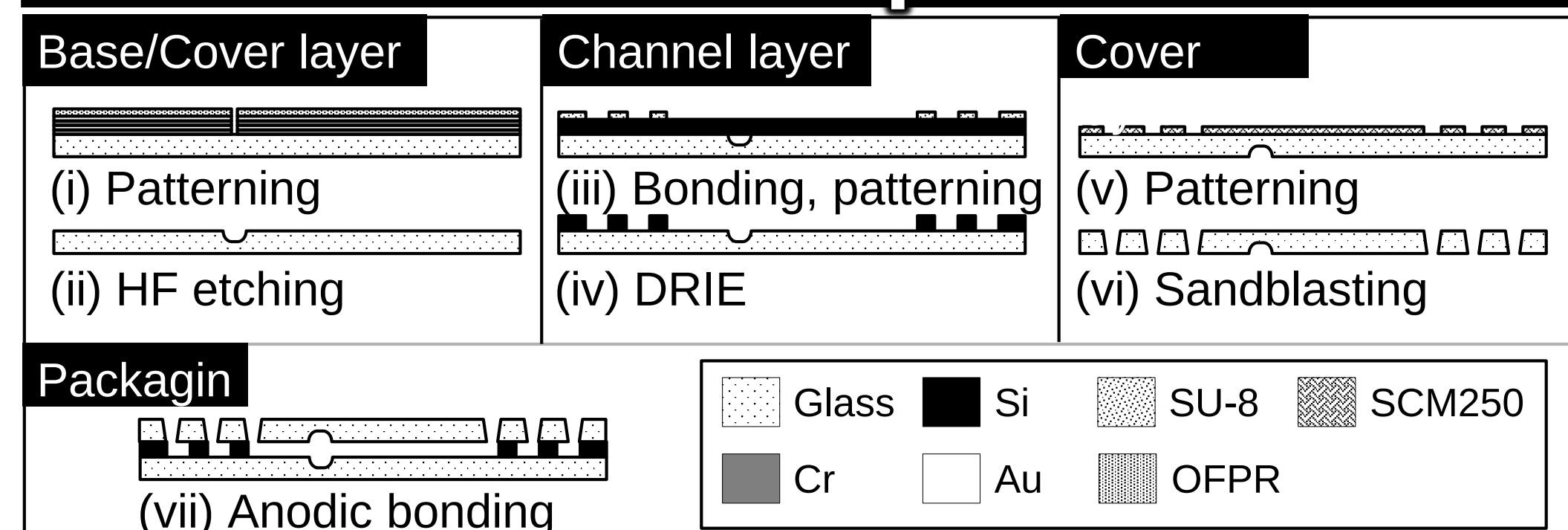
3D hydrodynamic focusing

Vertical sheath inlet
Horizontal sheath inlet
Sample inlet

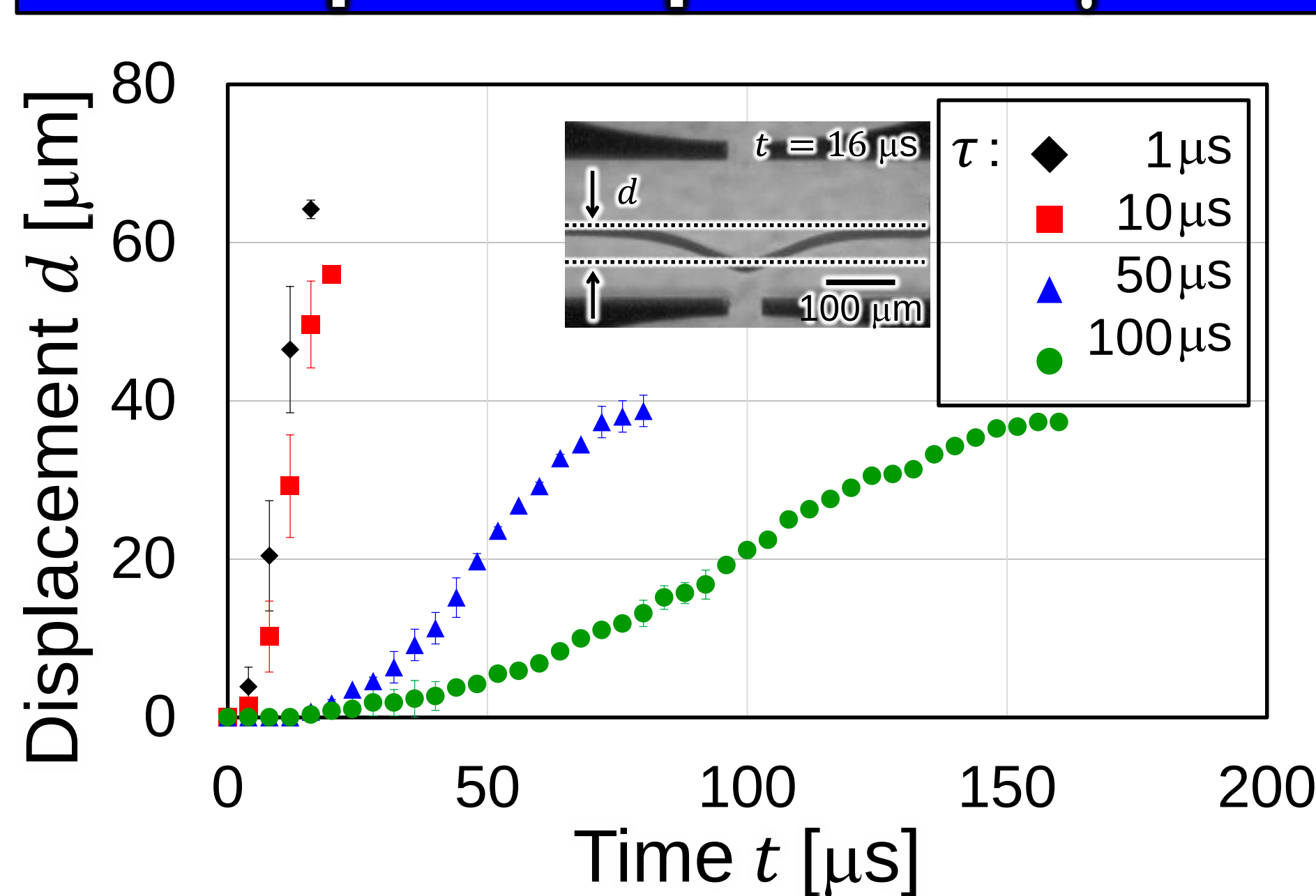
Principle of sorting



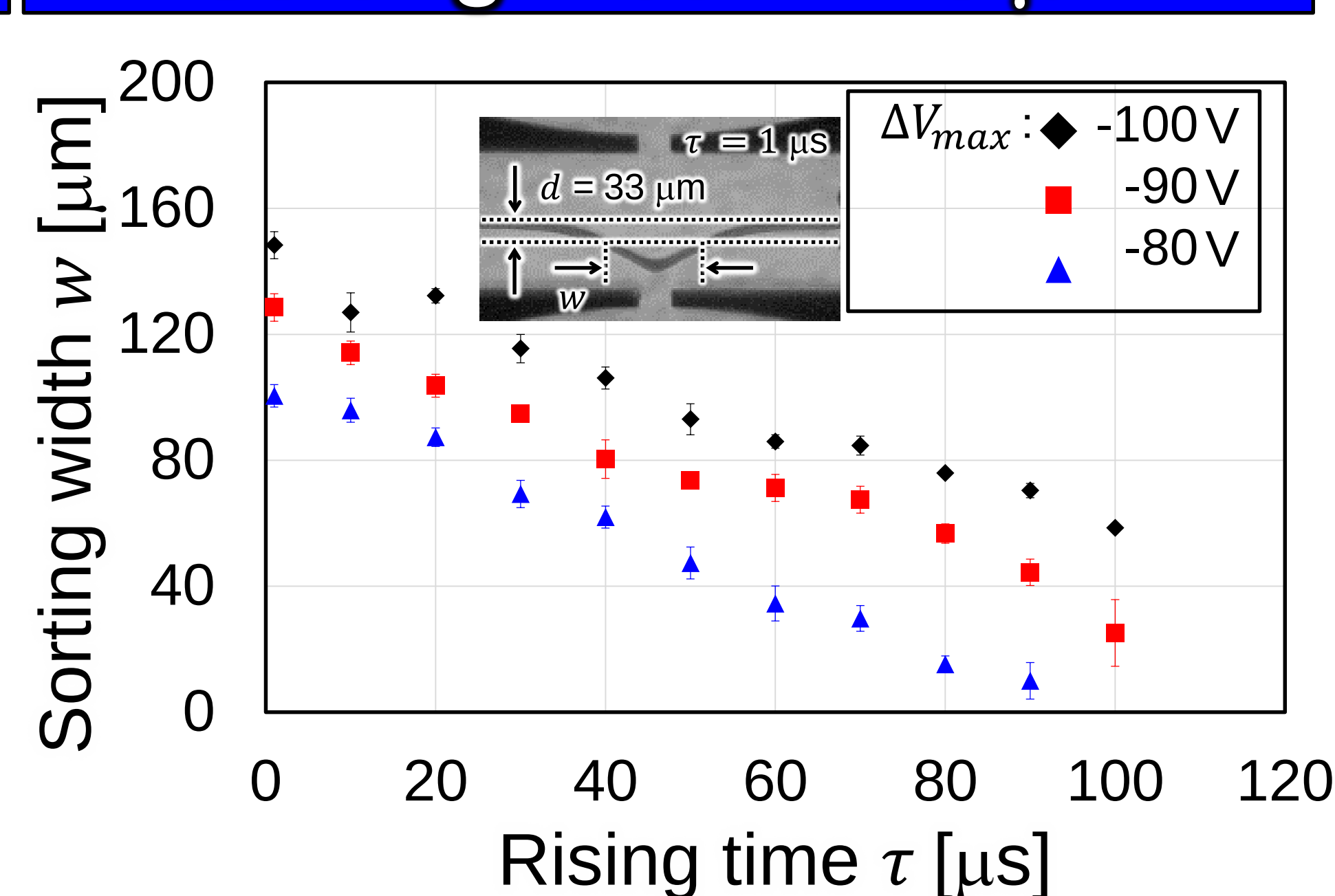
Fabrication process



Response speed : 16 μs

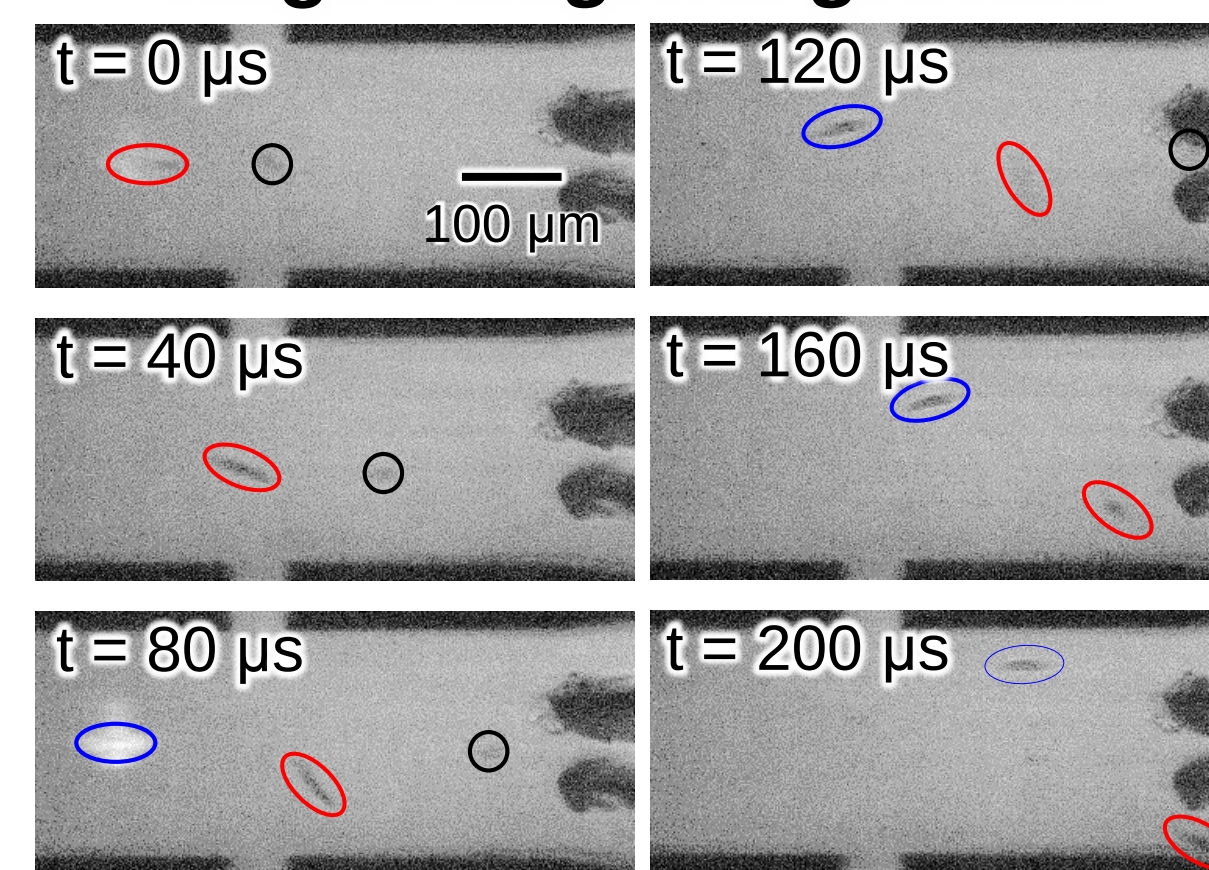


Sorting width : 148 μm



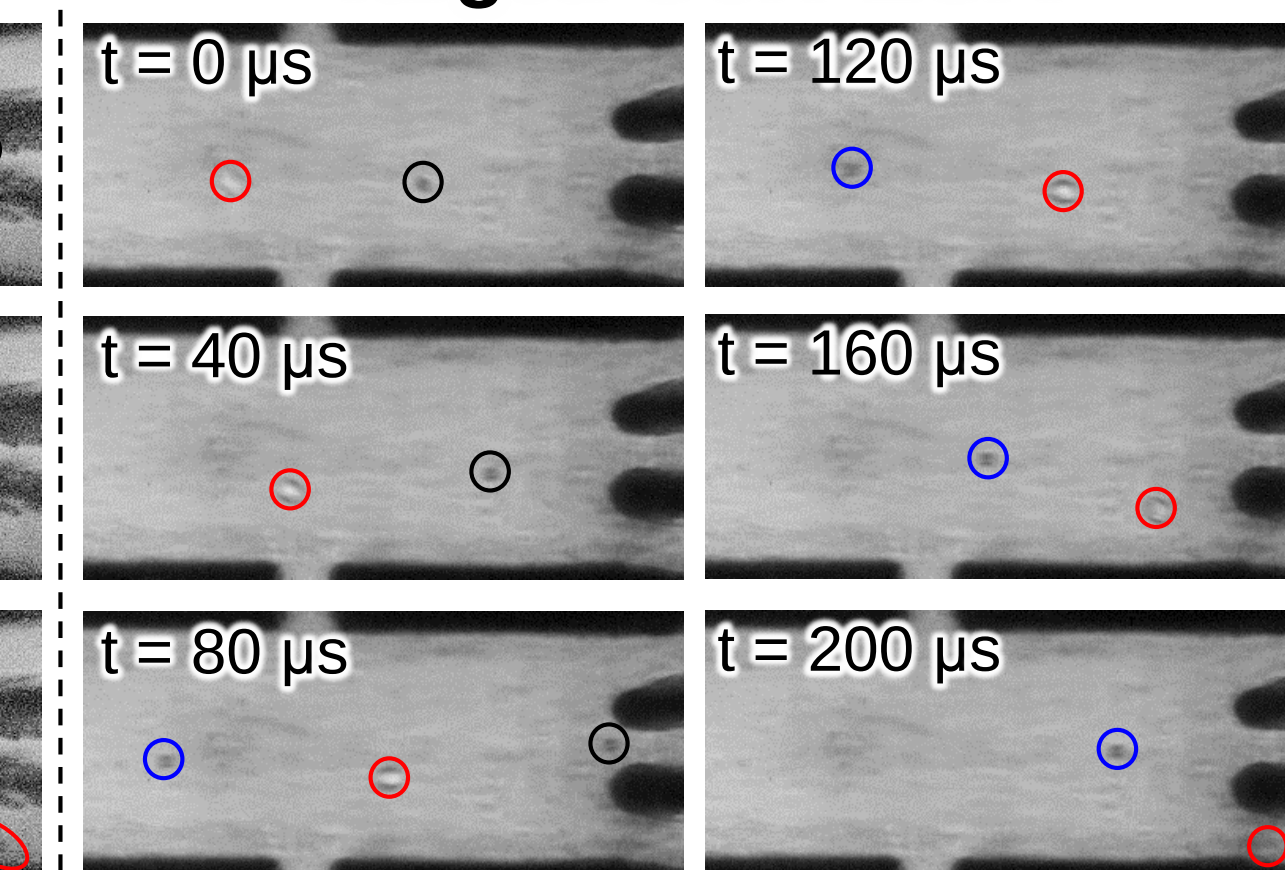
Experiments of on-chip cell sorting

Target: *Euglena gracilis*



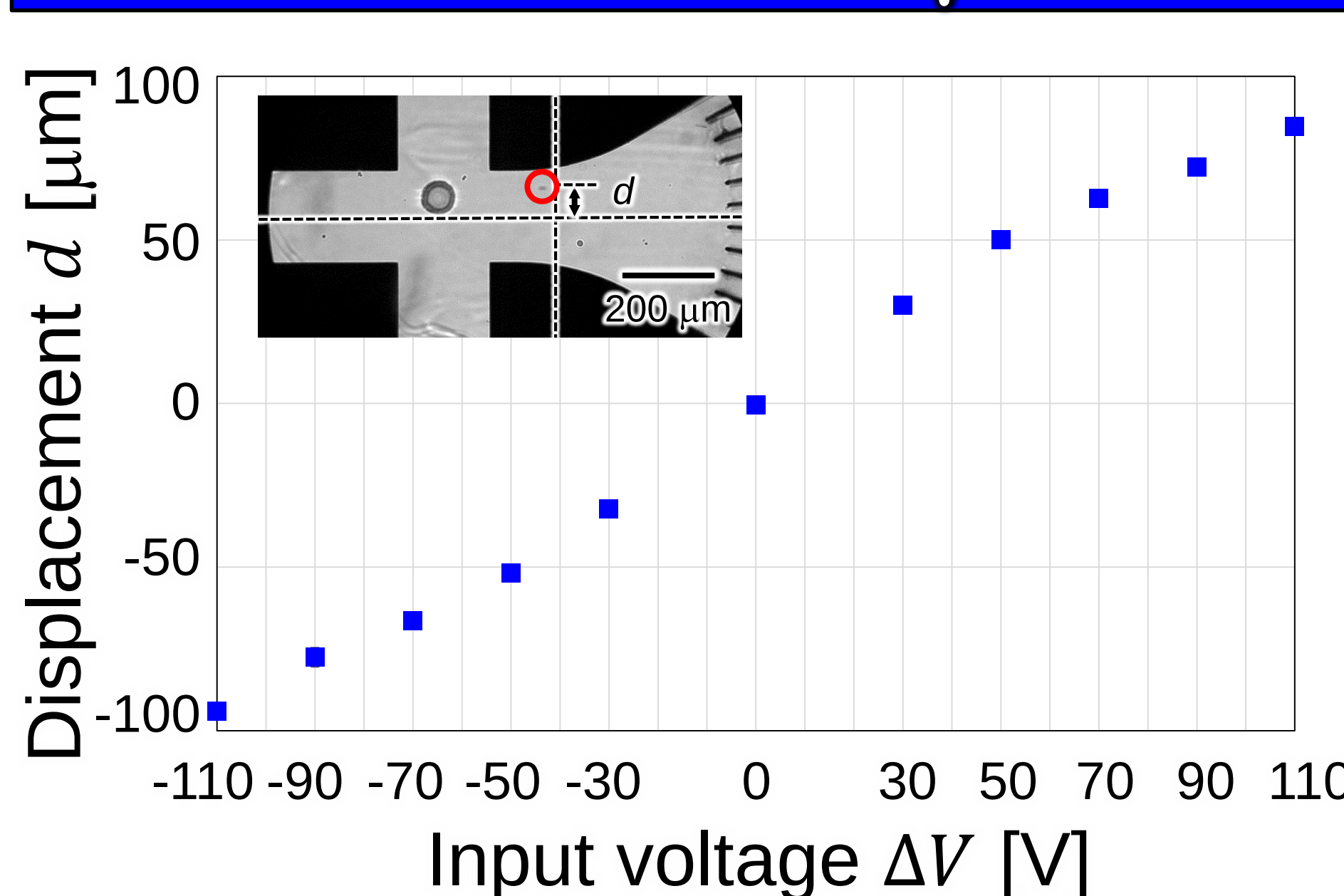
Max. event rate : 23 kHz
Success rate : 92.8%
Purity : 95.8%
Viability : 90.8 %

Target: GCY-EGFP

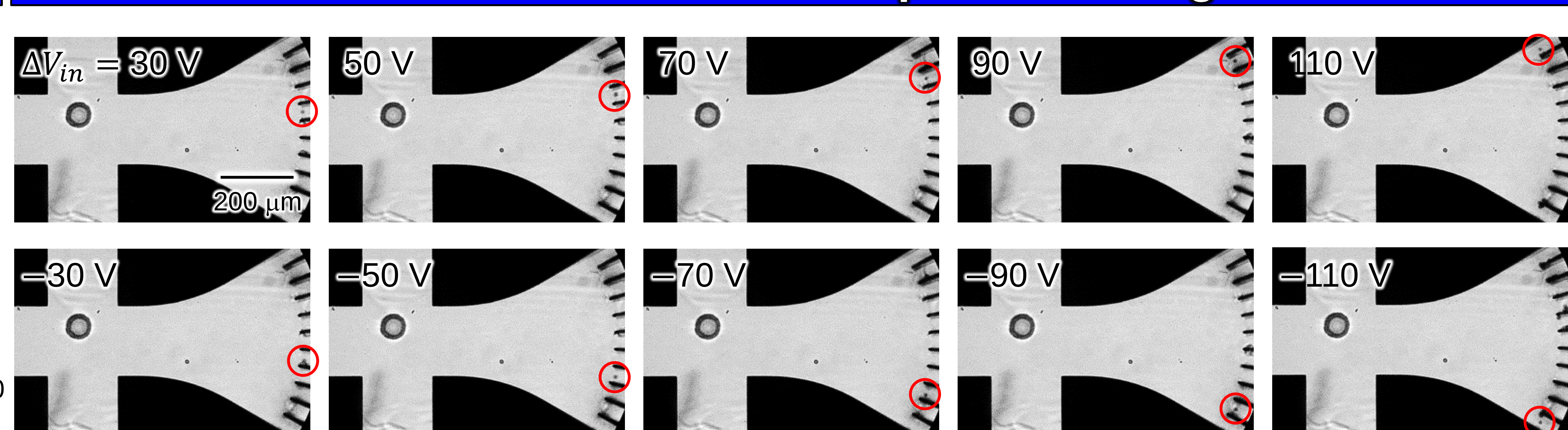


Max. event rate : 11 kHz
Success rate : 97.8%
Purity : 98.9%
Viability : 90.7 %

Precision : 3.0 μm



Demonstration of on-chip multi-sorting



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Reference :
S. Sakuma, Y. Kasai, T. Hayakawa, F. Arai, On-chip cell sorting by high-speed local-flow control using dual membrane pumps, Lab on a Chip, 17, 2760-2767, 2017, DOI:10.1039/c7lc00536a

